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ESD Protection Network Utilizing Precharge Bus Lines

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ESD PROTECTION NETWORK UTILIZING PRECHARGE BUS LINES

Technical Field

[0001] The present invention relates generally to electrostatic discharge (ESD) protection. More specifically, the present invention relates to an ESD protection device and method comprising a precharged bus line designed to protect the components of an integrated circuit and to prevent deleterious effects caused by undesirable transient currents during operation.

Background

[0002] Integrated circuits (ICs) may be severely damaged by electrostatic discharge (ESD) phenomena. An IC may be exposed to ESD from many sources. A major source of ESD exposure to ICs is the human body. A charge of about 0.6 microcoulombs can be induced on a body capacitance of 100pF, leading to electrostatic discharge potentials of 4 kV or greater. Any contact by a charged human body with a grounded object, such as a pad of an IC, can produce an electrostatic discharge with approximately a 10 nanosecond (ns) rise time and a discharge time of approximately 450 ns (i.e., the total discharge time is approximately equivalent to three time constants, where each time constant is approximately 150 nanoseconds), during which peak currents of several amps are input into the IC.

[0003] A second source of ESD is a metallic object. The metallic object ESD source model is characterized as having a greater capacitance and lower internal resistance than the human body model discussed above. Metallic objects produce ESD transient with approximately the same rise time as a human body discharge but the discharge rings as the nearly negligible resistance of the metallic object results in an underdamped condition.

[0004] A third source of ESD is a charge device, involving situations where the IC itself becomes charged and then discharged to ground. The charge device pulses have

very fast rise times (approximately one hundred picosecond) compared to those generated by a human body. The charge device current also rings with a short ringing interval of approximately one nanosecond.

[0005] A common ESD IC protection scheme uses a network of diodes or transistors and supply clamps to attempt to divert the potentially destructive energy of a static discharge around any sensitive internal circuitry. However, some circuit applications require signal pins of ICs to occasionally operate at voltages above the positive voltage supply (Vdd) or voltages below the negative supply voltage (Vss). The performance of internal circuitry protected by such an ESD protection scheme can become unreliable when signal pins are exposed to required positive or negative pulses that exceed normal operating voltage levels. This is generally due to parasitic currents that occur, through diodes or transistors incorporated in ESD protection schemes, when the voltage levels either exceed Vdd or are lower than Vss. The parasitic currents can degrade the operational signals and cause latch up problems in the ICs.

[0006] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an ESD protection scheme that is reliable even when required positive or negative voltage signals are applied to signal pins that exceed normal operating voltage levels.

Summary

[0007] The above-mentioned problems and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0008] In one embodiment, an electrostatic discharge protection circuit is disclosed. The electrostatic discharge protection circuit includes one or more electrostatic bus lines, a plurality of signal bonding pads and a charge pump for each electrostatic bus line. The one or more electrostatic bus lines are used to direct electrostatic discharge

around internal circuitry. The plurality of signal bonding pads are used to receive external voltage signals. Each signal bonding pad is coupled to an associated electrostatic bus line via an unidirectional conducting device. Each charge pump is used to precharge its associated electrostatic bus line to an associated predetermined voltage level. The pre-charging of each electrostatic bus line to its predetermined voltage level reduces transient currents on the signal bonding pads associated with capacitive charging of the electrostatic bus lines when the external voltage signals levels are beyond normal supply voltage ranges.

[0009] In another embodiment an integrated circuit comprises functional circuitry, first and second ESD bus lines, first and second charge pumps and first and second unidirectional conducting devices. The first ESD bus line is used to direct electrostatic discharge pulses away from the functional circuitry. The first charge pump is coupled to charge the first ESD bus line to a predetermined first voltage. The second ESD bus line is used to further direct electrostatic discharge pulses away from the functional circuitry. The second charge pump is coupled to charge the second ESD bus line to a predetermined second voltage. The first unidirectional conducting device is coupled between a first signal connection and the first ESD bus line. The second unidirectional conducting device is coupled between a second signal connection and the second ESD bus line. The first and second ESD bus lines are charged to their respective first and second voltage levels to reduce transient currents through the first and second unidirectional conducting devices when voltages applied to the first and second signal connections are outside the normal range of power supply operating voltages for the integrated circuit.

[0010] In another embodiment, an ESD protected integrated circuit comprises a positive ESD bus line, first and second signal bonding pads, a first unidirectional conducting device, a second bus line, a second unidirectional conducting device and a positive rail charge pump. The positive ESD bus line is used to route positive electrostatic discharge pulses around functional circuitry. The first and second signal

bonding pads are used to receive external voltage signals. The first unidirectional conducting device is coupled between the first signal bonding pad and the positive ESD bus line. The second bus line is coupled to selectively receive current from the positive ESD bus line. The second unidirectional conducting device is coupled between the second signal bonding pad and the second bus line. The positive rail charge pump is coupled to charge the positive ESD bus line to a predefined voltage level, wherein the predefined voltage level is higher than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting device during normal operations of the integrated circuit where voltage signals higher than a normal power supply operating voltage, but less than the predefined voltage signals, are applied to the first signal bonding pad.

[0011] In another embodiment, an ESD protected integrated circuit comprises a negative ESD bus line, first and second signal bonding pads, a first unidirectional conducting device, a second bus line, a second unidirectional conducting device and a negative rail charge pump. The negative ESD bus line is used to route negative electrostatic discharge pulses around functional circuitry. The first and second signal bonding pads are used to receive external voltage signals. The first unidirectional conducting device is coupled between the first signal bonding pad and the negative ESD bus line. The second bus line is coupled to selectively receive current from the negative ESD bus line. The second unidirectional conducting device is coupled between the second signal bonding pad and the second bus line. A negative rail charge pump is coupled to charge the negative ESD bus line to a predefined voltage level, wherein the predefined voltage level is lower than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting devices during normal operations of the integrated circuit where voltage signals lower than a normal power supply operating voltage, but more than the predefined voltage signals, are applied to the first signal bonding pad.

[0012] In another embodiment, a method of operating an integrated circuit that requires signal voltages outside the normal range of power supply operational voltages, the integrated circuit including an electrostatic discharge circuit having one or more electrostatic discharge bus lines. The method comprising, pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.

[0013] In another embodiment, a method of operating an integrated circuit having electrostatic discharge protection. The method comprising, coupling a positive ESD bus line to an integrated circuit to direct positive electrostatic pulses away from functional circuitry of the integrate circuit, pre-charging the positive ESD bus line to a predetermined positive voltage level, wherein the predetermined positive voltage level is above the voltage level of expected signals to be applied to the integrated circuit. Coupling a negative ESD bus line to the integrated circuit to direct negative electrostatic pulses away from the functional circuitry of the integrated circuit and pre-charging the negative ESD bus line to a predetermined negative voltage level, wherein the predetermined negative voltage level is below the voltage level of expected signals to be applied to the integrated circuit.

Brief Description of the Drawings

[0014] The present invention can be more easily understood and further advantages and uses thereof more readily apparent, when considered in view of the description of the preferred embodiments and the following figures in which:

[0015] Figure 1 is a schematic diagram of one embodiment of the present invention;

[0016] Figure 2A is a schematic diagram of one embodiment of a supply clamp of the present invention;

[0017] Figure 2B is a schematic diagram of another embodiment of a supply clamp of the present invention;

[0018] Figure 3 is a schematic diagram of one embodiment of a positive rail charge pump of the present invention;

[0019] Figure 4 is a schematic diagram of one embodiment of the present invention with a positive rail charge pump;

[0020] Figure 5 is a cross-sectional view of a portion of an integrated circuit of the present invention illustrating one embodiment of a transistor in a N well CMOS structure;

[0021] Figure 6 is a schematic diagram of one embodiment of the present invention with a negative rail charge pump; and

[0022] Figure 7 is a cross-sectional view of a portion of an integrated circuit of the present invention illustrating one embodiment of a transistor in a P well CMOS structure.

[0023] In accordance with common practice, the various described features are not drawn to scale but are drawn to emphasize specific features relevant to the present invention. Reference characters denote like elements throughout Figures and text.

Detailed Description

[0024] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims and equivalents thereof.

[0025] Embodiments of the present invention are described with reference to two voltages designated Vss and Vdd. Those skilled in the art recognize that these voltage references can be implemented from two separate voltage sources, or Vdd and Vss can be opposite terminals of a single voltage source. In any case, it is only the relationship between Vdd and Vss that is important; Vdd is the most positive voltage; Vss is the most negative voltage, i.e., Vdd is greater than Vss. Typically, Vdd is a positive value greater than zero and Vss is a negative value less than zero. But this is not necessary. Also, in many applications Vss is in fact ground potential, although again this is not always the case. In fact, Vdd can be at ground or zero potential and Vss would therefore be a negative voltage.

[0026] Referring to Figure 1, one embodiment of an ESD protected integrated circuit 100 of the present invention is illustrated. As illustrated, the ESD protected integrated circuit 100 includes a power supply (Vdd) bonding pad 12 and a power supply (Vss) bonding pad 18. The Vdd bonding pad 12 is coupled to receive Vdd. The Vdd bonding pad 12 is coupled to a first ESD bus line 45 by diode 40. In particular, the cathode terminal of diode 40 is coupled to the first ESD bus line 45 and the anode terminal of diode 40 is coupled to the Vdd bonding pad 12. In addition, Vdd bonding pad 12 is also coupled to a second ESD bus line 47 by diode 42. In particular, the cathode terminal of diode 42 is coupled to the Vdd bonding pad 12 and the anode terminal of diode 42 is coupled to the second ESD bus line 47. The Vss bonding pad 18 is coupled to receive Vss. In addition, Vss bonding pad 18 is coupled to the first ESD bus line 45 by diode 44. In particular, the cathode terminal of diode 44 is coupled to the first ESD bus line 45 and the anode terminal of diode 44 is coupled to the Vss bonding pad 18. Moreover, Vss bonding pad 18 is coupled to the second ESD bus line 47 by diode 46. In particular, the cathode terminal of the diode 46 is coupled to the Vss bonding pad 18 and the anode terminal of diode 46 is coupled to ESD bus line 47.

[0027] The ESD protected integrated circuit 100 has a first signal bonding pad 14 and a second signal bonding pad 22. The first signal bonding pad 14 can be referred to

as a first signal connection 14 and the second signal bonding pad 22 can be referred to as a second signal connection 22. The first signal bonding pad 14 is coupled to the first ESD bus line 45 by diode 10. In particular, the cathode terminal of diode 10 is coupled to the first ESD bus line 45 and the anode terminal of diode 10 is coupled to the first signal bonding pad 14. The first signal bonding pad 14 is also coupled to the second ESD bus line 47 by diode 16. In particular the cathode terminal of diode 16 is coupled to the first signal bonding pad 14 and the anode terminal of diode 16 is coupled to ESD bus line 47. The second signal bonding pad 22 is coupled to the first ESD bus line 45 with diode 20. In particular, the cathode terminal of diode 20 is coupled to the first ESD bus line 45 and the anode terminal of diode 20 is coupled to the second signal bonding pad 22. The second signal bonding pad 22 is also coupled to the second ESD bus line 47 by diode 24. In particular, the cathode terminal of diode 24 is coupled to the second signal bonding pad 22 and the anode terminal of diode 24 is coupled to the second ESD bus line 47.

[0028] The ESD protected integrated circuit 100 includes IC circuitry 28. The IC circuitry 28 is the internal functional circuitry of the integrated circuit and may be referred to as internal or functional circuitry 28. The IC circuitry performs the function of the integrated circuit 100. For example, the IC circuitry may be some type of processor, logic circuit or memory storage circuit. The present invention protects the IC circuitry 28 from the destructive energy of static discharges. As shown in Figure 1, the IC circuitry 28 is coupled to the anode terminal of diode 40 and the Vdd bonding pad 12. Moreover, the IC circuitry 28 is also coupled to the cathode terminal of diode 46, Vdd 12, diode 40, signal pads 14 and 22 and the Vss bonding pad 18. In addition, the first ESD bus line 45 can be referred to as the positive ESD bus line 45 and the second ESD bus line 47 can be referred as the negative ESD bus line 47. Also illustrated in Figure 1, is capacitance 50, which represents the capacitance of bus line 45 and capacitor 52, which represents the capacitance in of bus line 47.

[0029] In addition, as illustrated in Figure 1, the ESD protected integrated circuit 100 also includes a supply clamp 26 that is coupled between the positive and negative ESD bus lines 45 and 47. The supply clamp 26 is used to selectively conduct when an electrostatic pulse is detected. The supply clamp 26 can be referred to as a switching device 26. One embodiment of the supply clamp 26 of the present invention is illustrated in Figure 2A. As illustrated, the supply clamp 26 includes capacitor 30, resistor 32 and transistor 34. A first terminal of the capacitor 30 is coupled the positive ESD bus line 45 and a second terminal of capacitor 30 is coupled to node 35. Resistor 32 is coupled between node 35 and the negative ESD bus line 47. The base terminal of transistor 34 is coupled to node 35. The collector/emitter path of transistor 34 is coupled between the positive and negative ESD bus lines 45 and 47 as shown. In operation, as capacitor 30 is charged by an ESD pulse, transistor 34 turns on. The collector/emitter path then forms a low impedance path between the positive and negative ESD bus lines 45 and 47. During normal operations, the resistor 32 discharges node 35 thereby turning off the transistor 34. In other embodiments, the supply clamp 26 is implemented with a bipolar junction transistor, a MOSFET, a JFET, an SCR or any other device capable of conducting with low impedance to steer the ESD pulse around the IC circuitry 28. Such devices may be switched on by the fast rise time voltage of the ESD pulse or the voltage level of the ESD pulse. In still another embodiment, a zener diode may be used instead of the supply clamp 26. This may not be desired because zener diodes typically have a higher impedance than a collector/emitter path through the transistor 34.

[0030] However, in another embodiment of the supply claim 26, a zener diode 31 is used as a trigger as illustrated in Figure 2B. In this embodiment, the cathode of the zener diode 31 is coupled to the positive ESD bus line 45 and the anode of zener diode 31 is coupled to node 37. Resistor 32 is coupled between node 37 and the negative ESD bus line 47. The base terminal of transistor 34 is coupled to node 37. The

collector/emitter path of transistor 34 is coupled between the positive and negative ESD bus lines as shown in Figure 2B.

[0031] In operation, when a positive ESD pulse is detected form signal pad 14 to signal pad 22, the supply clamp 26 conducts. Thereafter, the ESD pulse is discharged through forward biased diode 10, ESD bus line 45, supply clamp 26, forward biased diode 24 and signal bonding pad 22. When a negative ESD pulse is detected the supply clamp 26 also conducts. The negative ESD pulse causes forward biasing of diode 16. This pulse is then discharged through forward biased diode 16, ESD bus line 47, supply clamp 26, ESD bus line 45 and finally through forward biased diode 20.

[0032] Referring back to Figure 1, the ESD protected integrated circuit 100 of this embodiment further has a positive rail charge pump 120 and a negative rail charge pump 122. The positive rail charge pump 120 is coupled between the Vdd bonding pad 12 and the positive ESD bus line 45. The negative rail charge pump 122 is coupled between the Vss bonding pad 18 and the negative bus line 47. The positive ESD bus line 45 is precharged to a voltage greater than the most positive expected input signal voltage by the positive rail charge pump 120. Similarly, the negative ESD bus line 47 is charged to a voltage below the most negative expected signal voltage by the negative rail charge pump 122.

[0033] The use of charge pumps 120 and 122 reduce the degradation of required operational voltage signals to the integrated circuit 100 that either exceed the positive Vdd or are less then the negative Vss. In particular, pre-charging the ESD bus lines 45 and 47 to their predetermined values reduces transient currents, associated with the charging of the capacitance of the ESD bus lines 45 and 47, on the signal bonding pads 14 and 22. When ESD bus lines 45 and 47 are pre-charged to the desired voltages, the steering diodes 10, 16, 20, 24, 40, 42, 44 and 46 remain in a reversed bias state during normal operations even if the voltage levels on the signal bonding pads 14 and 22 are beyond the normal range of the supply voltages. The steering diodes 10, 16, 20, 24, 40, 42, 44 and 46 may include Schottky diodes, vacuum diodes, junctions of bipolar

junction transistors or any other unidirectional conducting device. In the absence of the charge pumps 120 and 122, signal voltages in excess of Vdd or less than Vss would cause transient parasitic currents to flow through the ESD steering diodes 10, 16, 20 and 24 in charging the ESD bus lines 45 and 47. The parasitic currents could degrade the operational signals and cause latch up problems in the IC circuitry 28 thereby reducing the reliability of the IC circuitry 28.

[0034] Moreover, the charge pumps 120 and 122 are used to generate a respective second, reasonably stable, DC voltage from a respective first supply voltage. Advantageously, the DC circuit drive requirements of the charge pumps 120 and 122 are minimal, since the charge pumps 120 and 122 only have to provide a current to compensate for DC leakage currents of diodes 10, 16, 20, 24, 40, 42, 44 and 46 and the supply clamp 26. When the IC circuitry 28 is powered up, the charge pumps 120 and 122 are required to charge their respective bus lines (i.e., the positive ESD bus line 45 and the negative bus line 47, respectfully), to a desired voltage within a specified time. The desired voltage is chosen based on the application for the IC circuitry 28. In any case, the positive bus line 45 should be charged to a value greater than the highest expected signal voltage that will be applied to signal pad 14 or 22. Moreover, the negative bus line 47 should be charged to a value less than the lowest expected signal voltage that will be applied to signal pad 14 or 22. Generally, it is not difficult for the positive and negative rail charge pumps 120 and 122 to charge the bus lines as required because the Vdd and Vss supply voltages provide much of the initial charging current. Further, the duration of the power-up cycle is generally long enough to give the charge pumps adequate time to charge the positive and negative ESD bus lines 45 and 47 to the desired value. Generally, the time required to charge the ESD bus lines 45 and 47 will be between a few microseconds and a few milliseconds.

[0035] After the ESD bus lines 45 and 47 are precharged, according to the present invention, diodes 10, 16, 20, 24, 40, 42, 44 and 46, remain reversed biased when signal voltages between the positive precharge value of positive ESD bus line 45 and the

negative precharge value of negative ESD bus line 47 are input to the IC circuitry 28. Only capacitively-coupled transient currents from the input signals or ESD pulses and reverse bias leakage currents flow through the diodes 10, 16, 20, 24, 40, 42, 44 and 46. Since, it is known that the vast majority of the ESD pulses occur when the IC is not powered or functioning in an operational mode, the charging of the ESD bus lines 45 and 47 at power up does not hamper the electrostatic protection provided by the ESD protection device. In addition, during operational modes, when a positive ESD pulse having a voltage level higher than the voltage level of the positive ESD bus line 47 is applied between signal pads 14 and 22 the supply clamp 26 conducts. The positive ESD pulse is then discharged through forward biased diode 10, ESD bus line 45, supply clamp 26, forward biased diode 24 and signal bonding pad 22. Likewise, if a negative ESD pulse that has a voltage level below the negative ESD bus line is applied between signal bonding pads 14 and 22 the supply clamp also activates. The ESD pulse is then discharged through forward biased diode 16, ESD bus line 47, supply clamp 26, ESD bus line 45 and finally through forward biased diode 20.

[0036] Although, the embodiment illustrated in Figure 1 only shows two signal bonding pads 14 and 22 or signal connections 14 and 22, those skilled in the art will recognize that additional signal bonding pads are generally included with the IC circuitry 28 and that each additional signal bonding pad can be protected by the appropriate placement of diodes in a manner identical to the placement of diodes associated with signal bonding pads 14 and 22. Accordingly, the present invention is not limited to having only two signal pads.

[0037] An additional benefit of the use of charge pumps 120 and 122 in accordance with the present invention is the creation of a greater reverse bias voltage across diodes 10, 16, 20, 24, 40, 42, 44 and 46 during normal operations of the IC circuitry 28. The larger reverse bias voltage reduces the capacitance per area of the diodes (by increasing the depletion region width of each diode) and thus reduces the capacitivity-coupled

transient currents. Of course, the larger the reverse bias voltage requires that each diode have a corresponding higher reverse-breakdown voltage.

[0038] An embodiment of a positive rail charge pump 120 is illustrated in Figure 3. As illustrated, the positive rail charge pump has a first switch 154 that has a first side coupled to node A and a second side that is coupled to a first plate of a first capacitor 150. A second switch 156 has a first side also coupled to the first plate of the first capacitor 150 and a second side coupled to the positive terminal of power source 151 and to node B. A second capacitor 152 has a first plate coupled to the first side of the switch 154 and node A and a second plate coupled to the positive terminal of the power source 151 and node B. Also illustrated is third and fourth switches 158 and 160. The third switch 158 has a first side that is coupled to a second plate of capacitor 150 and a second side coupled the positive terminal of the power supply 151, node B and the second plate of capacitor 152. The fourth switch 160 has a first side coupled to the second plate of capacitor 150 and a second side coupled to a negative terminal of the power source 151 and node C. In particular, in the embodiment of Figure 3, each pair of switches (156 and 154) and (160 and 158) form a single pole double throw switch denoted as switches 171 and 173 respectively. As further illustrated by Figure 3, node A is coupled to the positive ESD bus line 45, node B is coupled to the Vdd bonding pad 12 and Node C is coupled to the Vss bonding pad 18.

[0039] In operation, assume initially, switches 154, 156, 158 and 160 are open and capacitors 150 (C1) and 152 (C2) are discharged. Closing switches 156 and 160 charges capacitor 150 (C1) to V1. Opening switches 156 and 160 and then closing switches 154 and 158 connects capacitor 150 (C1) in parallel with capacitor 152 (C1). The total charge initially stored on capacitor 150 (C1) equals C1V1. This charge redistributes when C1 is connected in parallel with C2 and the voltage across the capacitors becomes V1(C1/(C1+C2)). Switches 154 and 158 open and then switches 156 and 160 close, recharging capacitor 150 (C1) to V1. When switch 154 is open, capacitor 152 (C2) supplies the voltage between node A and B. Placing a load across

nodes A and C removes charge from capacitor 152 (C2). If the rate of charge removal from capacitor 152 (C2) by the load is small compared to the rate at which capacitor 150 (C1) supplies charge to capacitor 152 (C2), then the voltage across capacitor (C2) will approach V1 and the voltage from node A to node C will approach 2V1. To charge capacitors 150 (C1) and 152 (C2), switches 154 and 158 and switches 156 and 160 alternate between being open and close cycles, under the control of a control circuit (not shown). A negative charge pump can be similarly implemented. The charge pump of Figure 3 provides adequate voltage to prevent input signals from forward biasing the diodes 10, 20, 40 and 44 of Figure 1.

[0040] Referring to Figure 4, another embodiment of an ESD protection circuit 400 is illustrated. As illustrated, the ESD protection circuit 400 of this embodiment includes the positive rail charge pump 120 and transistors 130, 132 and 134. Each transistor 130, 132 or 134 can be referred to as a unidirectional conducting device. The positive rail charge pump 120 is coupled between the positive ESD bus line 45 and the Vdd bonding pad 12 and is used to precharge the positive ESD bus line 45. The emitter/collector path of transistor 134 is coupled between the Vdd bonding pad 12 and a first input 17 of the Vss bonding pad 18. The base terminal of transistor 134 is coupled to the positive ESD bus line 45. The emitter/collector path of transistor 130 is coupled between the first signal bonding pad 14 and the first input 17 of the Vss bonding pad 18. The base terminal of transistor 130 is coupled to the positive ESD bus line 45. The emitter/collector path of transistor 132 is coupled between the second signal bonding pad 22 and a second input 19 of the Vss bonding pad 18. The base terminal of transistor 132 is coupled to the positive ESD bus line 45.

[0041] Moreover, as Figure 4 illustrates, Vdd bonding pad 12 and Vss bonding pad 18 are coupled to the IC circuitry 28. In addition, the first signal bonding pad 14 and the second signal bonding pad 22 is also coupled to the IC circuitry 28. As illustrated, the supply clamp 26 is coupled between the positive ESD bus line 45 and the second

input 19 of the Vss pad 18. In addition, Vdd is coupled to the Vdd bonding pad 12 and Vss is coupled to the Vss bonding pad 18. Also illustrated is Vss bus line 21.

[0042] The charge pump 120 of the present invention is used to precharge the positive ESD bus line 45. This causes the base/emitter path of the transistor 130, 132 and 134 to be reversed biased. In operation, for example, if a positive polarity ESD pulse is applied between signal pads 14 and 22 of ESD protection circuit 400, a discharge current will start at signal pad 14 and flow through the now forward biased base/emitter diode of transistor 130 to the positive ESD bus line 45. The current will then flow through the supply clamp 26 to the Vss bus line 21. From there, the current will flow through forward biased diode 24 to signal pad 22. In addition to the aforementioned discharge path, another secondary path will also be taken by the discharge current. This secondary discharge path flows from signal pad 14 through the emitter/collector of transistor 130. Current passing through the base/emitter path allows the current through the emitter/collector path of transistor 130. The current then flows through the Vss bus line 21 and the forward biased diode 24 to signal pad 22.

[0043] Transistors 130, 132 and 134 in the embodiment of Figure 4 are created with a single well complementary metal oxide semiconductor (CMOS) N well process in an N well CMOS structure. A cross sectional view of a portion of the integrated circuit that contains the ESD protection integrated circuit 400 of Figure 4 is illustrated in Figure 5. In particular, Figure 5 illustrates transistor 130. As Figure 5 illustrates, a P+ source/drain diffusion 80 is formed in a N well diffusion 82. The P+ diffusion 80 and the N well diffusion 82 together with the underlying P substrate 84, form the vertical parasitic PNP transistor 130. Figure 5 also illustrates diode 16. Diode 16 is formed by placing an N+ source/drain diffusion 88 into the P substrate. In addition, transistors 134 and 132 and diodes 42 and 24 are formed in the same manner in the ESD protection integrated circuit 400 as transistor 130 and diode 16 are formed. A limitation of the embodiment of Figure 4 is that a negative ESD bus line cannot be implemented because Vss is connected to the P substrate. Therefore the ESD protection integrated circuit 400

of Figure 4, can provide parasitic current protection under those applications where the signal bonding pads 14 and 22 operate at voltages higher than Vdd but not at voltages lower than Vss. In particular, in this embodiment parasitic currents thru transistor 130 will be reduced during normal operations of the integrated circuit 400 where voltage signals higher than a normal operating voltage, but less than the predefined voltage signals, are applied to the first signal bonding pad 14.

[0044] The benefits of using charge pumps is more pronounced when a parasitic transistor such as transistor 130 of Figure 4 and Figure 5 is used as opposed to when just a diode is used. Any parasitic current that flows through the base/emitter of the transistor 130 to charge the positive bus line 45 will cause the emitter/collector current to flow from 14 to 17. This means a small ESD bus line charging current can cause a much larger (beta times) current to flow in the substrate 84. Relatively large substrate currents can lead to latch-up which can cause reliability problems.

[0045] In another embodiment, a single well CMOS P well structure is used to form an ESD protected integrated circuit 600 that protects against voltages lower than Vss. This embodiment is illustrated in Figure 6. As illustrated, the ESD protection circuit 600 includes the negative rail charge pump 122 and transistors 602, 604 and 606. The negative rail charge pump 122 is coupled between the negative ESD bus line 47 and the Vss bonding pad 18 and is used to precharge the negative ESD bus line 47. The collector/emitter path of transistor 606 is coupled between the Vss bonding pad 18 and a first input 13 of the Vdd bonding pad 12. The base terminal of transistor 606 is coupled to the negative ESD bus line 47. The collector/emitter path of transistor 604 is coupled between the second signal bonding pad 22 and the first input 13 of the Vdd bonding pad 12. The base terminal of transistor 604 is coupled to the negative ESD bus line 47. The collector/emitter path of transistor 602 is coupled between the first signal bonding pad 14 and a second input 15 of the Vdd bonding pad 12. The base terminal of transistor 602 is coupled to the negative ESD bus line 47.

[0046] Moreover, as Figure 6 illustrates, Vdd bonding pad 12 and the Vss bonding pad 18 are coupled to the IC circuitry 28. In addition, the first signal bonding pad 14 and the second signal bonding pad 22 are also coupled to the IC circuitry 28. As illustrated, the supply clamp 26 is coupled between the negative ESD bus line 47 and the first input 13 of the Vdd pad 12. In addition, Vdd is coupled to the Vdd bonding pad 12 and Vss is coupled to the Vss bonding pad 18. Also illustrated in Figure 6 is Vdd bus line 23.

[0047] Negative charge pump 122 of the present invention is used to precharge the negative ESD bus line 47. This causes the base/emitter path of the transistors 602, 604 and 606 to be reversed biased. In operation, for example, if a negative polarity ESD pulse is applied between signal pads 14 and 22 of ESD protection circuit 600, a discharge current will start at signal pad 22 and flow through the now forward biased diode 20 to Vdd bus line 23. The current will then flow through supply clamp 26 to the negative ESD bus line 47. The current will then flow through the now forward biased base/emitter path of transistor 602 to signal pad 14. In addition to the aforementioned discharge path, another secondary path will also be taken by the discharge current. This secondary path flows from signal pad 22 through forward biased diode 20 to Vdd bus line 23. Current then flows through the collector/emitter path of transistor 602 to signal pad 14. Current passing through the base/emitter path of transistor 602 allows the current through the collector/emitter path of transistor 602.

[0048] Transistors 602, 604 and 606 in the embodiment of Figure 6 are created with a single well CMOS P well process in an P well CMOS structure. A cross sectional view of a portion of the integrated circuit that contains the ESD protection integrated circuit 600 of Figure 6 is illustrated in Figure 7. In particular, Figure 7 illustrates transistor 604. As Figure 7 illustrates, a N+ source/drain diffusion 710 is formed in a P well diffusion 712. The N+ diffusion 710 and the P well diffusion 712 together with the underlying N substrate 714, form the vertical parasitic NPN transistor 604. Figure 7 also illustrates diode 20. Diode 20 is formed by placing an P+ source/drain diffusion

716 into the N substrate 714. In addition, transistors 602 and 606 and diodes 10 and 44 are formed in the same manner in the ESD protection integrated circuit 600 as transistor 604 and diode 20 are formed. A limitation, of the embodiment of Figure 6 is that a positive ESD bus line cannot be implemented because Vdd is connected to the N substrate. Therefore the ESD protection integrated circuit 600 of Figure 6, can provide parasitic current protection under those applications where the signal bonding pads 14 and 22 operate at voltages lower than Vss but not at voltages higher than Vdd. In particular, in this embodiment, parasitic currents thru transistor 602 will be reduced during normal operations of the integrated circuit 600 where voltage signals lower than a normal operating voltage, but more than the predefined voltage signals, are applied to the first signal bonding pad 14.

[0049] Although, Figures 4 and 6 both illustrate a single–well CMOS structure that limits the embodiments illustrated in Figures 4 and 6 to protect against parasitic currents when voltage signals are applied to signal connections that are either over Vdd or lower than Vss, it will be understood in the art that a twin-well CMOS structure could be implemented wherein both N type and P type wells are created in a P type or N type substrate, with appropriate isolation between the two wells. In this embodiment, internal circuitry will be protected from parasitic currents due to voltage levels exceeding Vdd as well as voltage level being below Vss being applied to signal connections.

[0050] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.